

Notice of References Cited	Application/Control No. 10/706,438		Applicant(s)/Patent Under Reexamination PARTSCH, TORSTEN	
	Examiner Kaushikkumar Patel		Art Unit 2188	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,187,686 A	02-1993	Tran et al.	365/189.11
*	B	US-5,500,818 A	03-1996	Chang et al.	365/189.05
*	C	US-5,959,899 A	09-1999	Sredanovic, Nikolas	365/189.02
*	D	US-5,999,458 A	12-1999	Nishimura et al.	365/189.05
*	E	US-7,184,508 B2	02-2007	Emberling, Brian D.	375/372
*	F	US-7,330,991 B2	02-2008	Au, Jonson C.	713/400
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
	U	Saeki et al. (A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay, published by IEEE journal of solid state circuits, vol. 31, November 1996), pages 1656-1668			
	V	Akioka et al. (A 6-ns 256-kb BiCMOS TTL SRAM, published by IEEE Journal of solid-state circuits, vol. 26, March 1991) pages 439-443			
	W				
	X				

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.